In the Specification

Amend the following numbered paragraphs of the specification:
(The only change to paragraph 0005 immediately below is that the period after "MHz" has been stricken.)

[0005] Improvements in semiconductor processing technology has enabled logic components such as microprocessors to operate at clock rates in excess of 3 GHz. Memory system clock rates have not kept pace because of the nature of DRAM memory devices. In order to perform well with these higher speed processors, synchronous dynamic random access memories (SDRAMs), operable with clock rates of up to 266 MHz and data rates of up to 533 M Bits per second, have been designed. SDRAMs are responsive to a high frequency clock signal generated by the system clocking circuitry often running at a clock multiple versus the processor, which renders all internal activity within the memory "synchronous" with other devices responsive to the same (or related) clock signal(s). In the synchronous approach, all SDRAM address and control inputs are sampled at the positive edge of the input clock, and all SDRAM outputs on recent DDR (Double Data Rate) SDRAMs are valid on subsequent positive and negative edges. This technique permits input/output transactions to take place on every clock cycle. SDRAMs can simplify both the overall system design and the memory-management subsystem, because the main memory operates in a deterministic, synchronous nature relative to the system clock.

[0006] As frequencies increase and cycle times decrease, memory designers are looking for additional ways to improve memory performance and timing margins. One element that can be improved is the timing ~~adder~~ latency component due to the simultaneous switching affect of all the drivers to the SDRAMs switching in the same direction at the same time. This delay contribution is known as simultaneous switch time (tSS). In recent low cost designs, this delay adder for tSS was as much as 1.06ns. This contribution was 14% of the total timing budget for a memory subsystem running at a 7.5ns cycle time.

[0007] Solutions to reduce the simultaneous switching delay adder include higher priced packaging, splitting the function across several components or running the memory at an increased cycle time.

[0008] Increased number of address/command signals due to larger DRAM or module densities only add to the simultaneous switching ~~timing~~ time delays for high performance/low cost memory solutions. The price tag for two single 14 bit 1:2 registers is usually less than about $2.00.

[0009] Furthermore, the concept of driving buses with half of the drivers providing non-inverting polarities and the other half of the drivers providing inverted polarities is a known way of reducing simultaneous switching affects. But this technique does not cover devices receiving those signals to accept the inverted signal polarity and still function as if they received the non-inverted signal polarity.

[0013] An example of the simultaneous switch impact is evident in the timing analysis (known as post-register timing analysis) on a Double Data Rate (DDR) SDRAM Registered DIMM (Dual Inline Memory Module), which consists of DDR SDRAMs, a PLL for clock distribution on the module and one or more registers that latch and re-drive the address and command signals from the system memory controller to the SDRAMs (Synchronous DRAMs). The simultaneous switching push-out due to the drivers internal to the register switching at the same time has been as large as 700ps at a cycle time of 10ns (JEDEC Standard PC100 Registered DIMM). With current designs, the simultaneous switch push-out has been reduced to approximately 300ps at a cycle time of 3.75ns, but this continues to be approximately 7-8% of the timing budget. This simultaneous switch noise could be reduced by improving the register package, by further splitting the register function across multiple devices, or by reducing the memory load, and each has been leveraged to the acceptable cost/performance limit for the current technology. The present invention provides an alternate solution, whereby the DRAM itself is designed to operate with non-inverted or inverted address and command inputs.

[0016] It should also be understood that increased package density and/or reductions in the area allocated to the memory subsystem will result in increased simultaneous switching affects, as more outputs on ~~less~~ fewer packages will be switching, and current methods will not serve to decrease the number and combinations of outputs switching at a given time. The proposed solution may provide only a small benefit (10-20%) in applications with several re-drive devices, but a very sizeable benefit (50% or greater) in applications with a single re-drive device and a large number of inputs and outputs. Current plans for DDR II server memory subsystems include low-cost registers with 28 inputs and 2 to 3 output copies.

[0025] Others have had to go with more complex and expensive packaging to reduce the simultaneous noise, or have used additional components to spread the function across multiple devices. The present invention reduces the maximum count of drivers that will be switching in ~~anyone~~ any one direction at a time, by utilizing a memory device that is designed to accept inverted inputs when so programmed. This invention will not add complexity or cost to either part, and the performance benefit gained will exceed the minimal delay impact that might occur in the memory or register device. In addition, this design decreases the min/max timing variation (spread) for all possible output signal combinations, thereby increasing the valid window of time for these signals at the receiving device. Independent of all other factors, increasing the valid window for these signals will permit higher frequency operation.